

	L #	Hits	Search Text	DBs
1	L1	28267	stack near10 (frame area region space)	USPAT; US-PGPUB
2	L2	285	(bit field tag flag cod\$3 encod\$3) near10 (sav\$3 stor\$3) near15 1	USPAT; US-PGPUB
3	L3	12095	stack near10 (frame area region space)	EPO; JPO; DERWENT; IBM_TDB
4	L4	74	(bit field tag flag cod\$3 encod\$3) near10 (sav\$3 stor\$3) near15 3	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	JP 20032 88129 A	<input type="checkbox"/>	MEMORY MANAGEMENT METHOD, MEMORY DEVICE, COMPUTER SYSTEM, COMPILER AND PROGRAM	
2	JP 20022 53821 A	<input type="checkbox"/>	GAME MACHINE	
3	JP 20020 41326 A	<input type="checkbox"/>	CENTRAL PROCESSING UNIT TO FACILITATE TEST AND DEBUGGING OF PROGRAM	
4	JP 20013 53267 A	<input type="checkbox"/>	GAME MACHINE	
5	JP 20022 53821 A	<input type="checkbox"/>	GAME MACHINE	
6	JP 20020 41326 A	<input type="checkbox"/>	CENTRAL PROCESSING UNIT TO FACILITATE TEST AND DEBUGGING OF PROGRAM	
7	JP 20013 53267 A	<input type="checkbox"/>	GAME MACHINE	
8	JP 20002 52445 A	<input type="checkbox"/>	MANUFACTURE OF INTEGRATED CIRCUIT ELEMENT	
9	JP 20002 22242 A	<input type="checkbox"/>	METHOD AND DEVICE FOR COMPILATION AND METHOD AND DEVICE FOR STACK TRACING	
10	JP 11085 531 A	<input type="checkbox"/>	LANGUAGE PROCESSOR AND STORAGE MEDIUM RECORDING PROGRAM REALIZING LANGUAGE PROCESSOR	
11	JP 10083 305 A	<input type="checkbox"/>	DATA PROCESSING SYSTEM WITH SELF-MATCHING STACK POINTER AND ITS METHOD	
12	JP 09231 133 A	<input type="checkbox"/>	CACHE MEMORY DEVICE	
13	JP 07160 497 A	<input type="checkbox"/>	MICROCOMPUTER	
14	JP 06290 053 A	<input type="checkbox"/>	CHARACTER-STRING CONSTANT LEXICAL ANALYZING SYSTEM	
15	JP 06152 692 A	<input type="checkbox"/>	CODING PROCESSING UNIT	
16	JP 05181 712 A	<input type="checkbox"/>	STACK HISTORY FORMING SYSTEM	
17	JP 05006 281 A	<input type="checkbox"/>	INFORMATION PROCESSOR	
18	JP 04334 182 A	<input type="checkbox"/>	PICTURE INPUT DEVICE	
19	JP 04040 530 A	<input type="checkbox"/>	REAL TIME PROCESSOR	
20	JP 03218 529 A	<input type="checkbox"/>	HIGH SPEED INTERRUPTION PROCESSOR	

	Document ID	U	Title	Current OR
21	JP 03211 687 A	<input type="checkbox"/>	DATA TRANSFER CIRCUIT	
22	JP 03204 036 A	<input type="checkbox"/>	COMPUTER WITH DYNAMIC RESTART MECHANISM AFTER INTERRUPTION PROCESSING	
23	JP 03075 940 A	<input type="checkbox"/>	MULTITASK CONTROLLER	
24	JP 02217 947 A	<input type="checkbox"/>	DATA PROCESSOR	
25	JP 02156 342 A	<input type="checkbox"/>	PROGRAM DEBUGGING SYSTEM	
26	JP 02141 842 A	<input type="checkbox"/>	MEMORY AREA REUSE PROCESSING SYSTEM	
27	JP 02077 841 A	<input type="checkbox"/>	BACKTRACKING PROCESSING SYSTEM WITH LOGIC TYPE LANGUAGE	
28	JP 01112 339 A	<input type="checkbox"/>	CODE MANAGING SYSTEM	
29	JP 01111 239 A	<input type="checkbox"/>	ERROR DISPLAY SYSTEM	
30	JP 01041 934 A	<input type="checkbox"/>	METHOD FOR PROCESSING STACK OF PROLOG MACHINE	
31	JP 63273 946 A	<input type="checkbox"/>	DATA LOADING PROCESSOR	
32	JP 63255 704 A	<input type="checkbox"/>	ARITHMETIC SYSTEM FOR SEQUENCER	
33	JP 63047 843 A	<input type="checkbox"/>	INTERRUPTING SYSTEM FOR PROCESSING IN EXECUTION	
34	JP 62140 136 A	<input type="checkbox"/>	DATA MEMORY DEVICE	
35	JP 62069 332 A	<input type="checkbox"/>	STORING SYSTEM FOR HISTORY INFORMATION	
36	JP 61248 152 A	<input type="checkbox"/>	PROCEDURE CHANGE CONTROLLING SYSTEM	
37	JP 61235 928 A	<input type="checkbox"/>	KEY INPUTTING SYSTEM	
38	JP 61216 012 A	<input type="checkbox"/>	PROCESSING SYSTEM FOR HIT OF POWER SUPPLY	
39	JP 61213 902 A	<input type="checkbox"/>	NC DEVICE WITH AUTOMATIC THREE-DIMENSIONAL PROGRAMMING FUNCTION	
40	JP 61210 480 A	<input type="checkbox"/>	FORMATION DATA MEMORY AND PROCESSING SYSTEM IN CAD/CAM SYSTEM	
41	JP 61136 128 A	<input type="checkbox"/>	CONTROL PROCESSING SYSTEM CAPABLE OF REENTRANT OF PROGRAM	
42	JP 61131 130 A	<input type="checkbox"/>	REGISTER SAVING METHOD	
43	JP 61029 943 A	<input type="checkbox"/>	STACK CONTROL SYSTEM	

	Docum ent ID	U	Title	Current OR
44	JP 60105 062 A	<input type="checkbox"/>	STACK CONTROL METHOD	
45	JP 59165 145 A	<input type="checkbox"/>	POINTER	
46	JP 59117 622 A	<input type="checkbox"/>	TEXT INPUT CONTROLLING SYSTEM	
47	JP 57174 743 A	<input type="checkbox"/>	INTERRUPTION PROCESSING CIRCUIT	
48	JP 57034 250 A	<input type="checkbox"/>	PROGRAM CONTROLLING SYSTEM	
49	JP 56094 405 A	<input type="checkbox"/>	SEQUENCE CONTROLLER	
50	JP 54074 649 A	<input type="checkbox"/>	STACK CONTROL MECHANISM	
51	EP 80248 1 A1	<input type="checkbox"/>	A data processing system having a self-aligning stack pointer and method therefor	
52	US 20030 13584 7 A	<input type="checkbox"/>	Instrumented process reverting method in PC, cell phone, involves determining storage location of return pointer in call stack of process, and changing its value from instrumented code space to uninstrumented code space.	
53	US 20030 00738 4 A	<input type="checkbox"/>	Non-volatile semiconductor memory e.g. EEPROM comprises stacked field effect transistors storing data of multibits and address space allocated in fixed position	
54	JP 20002 22242 A	<input type="checkbox"/>	Compilation of Java program in network computing, involves storing address of execution code which changes stack pointer and information about size of stack frame after change, in memory	
55	US 60386 11 A	<input type="checkbox"/>	API method for user-to-network interface signaling in ATM networks provides intelligent and flexible programming interface enabling higher layer software to set up and tear down ATM connections more efficiently	
56	US 59566 29 A	<input type="checkbox"/>	Transmitter selection apparatus for mobile transmission within service area for vehicle	
57	US 59095 79 A	<input type="checkbox"/>	Live pointer location encoding method in program data stack frame for computer system	
58	RD 41708 1 A	<input type="checkbox"/>	Calling 64-bit functions from 32-bit functions - involves converting 32-bit registers to 64-bit, and changing processor mode of operation from 32-bit to 64-bit	
59	JP 10340 228 A	<input type="checkbox"/>	Cache control system for microprocessor - prohibits replacement of stack area with respect to corresponding tag	
60	JP 10312 293 A	<input type="checkbox"/>	Program development assistance apparatus - has conversion unit which converts read code into certain format which is then stored in stack area of memory, when converted format of each block is not matched with predefined information	
61	US 58325 26 A	<input type="checkbox"/>	Tagging method for random access storage device - involves determining presence and amount of storage stack space in locally last storage sub-area, based on which end of file tagging code is recorded in that space	
62	KR 93088 83 B	<input type="checkbox"/>	Stack capacitor mfr. - comprises patterning three layers of oxide, nitride and oxide and forming poly:silicon storage nodes	
63	KR 93007 17 B	<input type="checkbox"/>	DRAM with stacked capacitor - includes V-shaped active region with bit line contact at vertex and storage node contacts at branch ends for honeycomb structure NoAbstract	

	Document ID	U	Title	Current OR
64	EP 49297 0 A	<input type="checkbox"/>	Extending computer architecture from thirty-two to sixty-four bits - reviewing indication designating word size in registers each time restore operation occurs to determine size of word in procedure being restored	
65	JP 04161 191 A	<input type="checkbox"/>	Appts. to control speed of sewing machine drive motor - has RAM to store data for control mode of motor, speed setting, stitch number, embroidery data, etc., read from floppy disc	
66	US 50348 86 A	<input type="checkbox"/>	Computer system for reducing number of dedicated registers - using memory stock and sharing of address and general purpose registers wholly or partly composed of wide use register	
67	EP 43723 5 A	<input type="checkbox"/>	Stacking system of single chip microcomputer - has stack area addressable to store 12 bit or 4 bit words changing assignment of data to RAM address according to commands	
68	KR 91019 83 B	<input type="checkbox"/>	Mfg. DRAM cell having trench-type and stack-type capacitors - is provided with mini-field oxide for connecting storage and source regions	
69	RD 30900 5 A	<input type="checkbox"/>	Placement of random logic macro in CMPHILO bit stack - enhances efficiency of max. functions on chip when signals to macro are vertically contained in stack	
70	US 46939 49 A	<input type="checkbox"/>	Universal storage battery housing for e.g. automobile - has peripheral frame engaging periphery of top wall of battery and central bail overlying medial portion of top wall	
71	US 44357 80 A	<input type="checkbox"/>	Separate stack areas for several process - uses process control block with link field to form distributed list of processes in despatching priority order	
72	DE 31100 81 A	<input type="checkbox"/>	Print viewing and storage frame - has slider with plastics moulded spring tags to extract print and return it to top of stack	
73	CH 61697 9 A	<input type="checkbox"/>	Extendable transportable building used as field hospital - is equipped with stacking beds stored in roof during transit, sanitary blocks and emergency operating area	
74	US 40683 03 A	<input type="checkbox"/>	Address translation managing system with translation pair purging - has buffer storage device swiftly translating logical address into corresponding real address	

	Document ID	U	Title	Current OR
1	US 20040 04735 3 A1	<input type="checkbox"/>	Frame transfer method and node in network, and frame transfer program	370/395 .63
2	US 20040 04226 8 A1	<input type="checkbox"/>	ONE-DEVICE NON-VOLATILE RANDOM ACCESS MEMORY CELL	365/185 .08
3	US 20040 01592 7 A1	<input type="checkbox"/>	Percolating hot function store/restores to colder calling functions	717/155
4	US 20040 01075 4 A1	<input type="checkbox"/>	System and method for transformation of XML documents using stylesheets	715/513
5	US 20040 00337 7 A1	<input type="checkbox"/>	Converting byte code instructions to a new instruction set	717/136
6	US 20030 22602 2 A1	<input type="checkbox"/>	Secure execution mode exceptions	713/189
7	US 20030 22601 4 A1	<input type="checkbox"/>	Trusted client utilizing security kernel under secure execution mode	713/164
8	US 20030 22108 5 A1	<input type="checkbox"/>	Implementation of thread-static data in multi-threaded computer systems	711/220
9	US 20030 21863 2 A1	<input type="checkbox"/>	Method and architecture of an event transform oriented operating environment for a personal mobile display system	345/740
10	US 20030 21732 7 A1	<input type="checkbox"/>	Compiling method with exception handling	714/798
11	US 20030 21298 8 A1	<input type="checkbox"/>	Preserving program context when adding probe routine calls for program instrumentation	717/130
12	US 20030 20975 4 A1	<input type="checkbox"/>	Two bit non-volatile electrically erasable and programmable memory structure, a process for producing said memory structure and methods for programming, reading and erasing said memory structure	257/314
13	US 20030 17364 3 A1	<input type="checkbox"/>	Silicide-silicon oxide-semiconductor antifuse device and method of making	257/530
14	US 20030 17229 3 A1	<input type="checkbox"/>	System and method of foiling buffer-overflow and alien-code attacks	713/200
15	US 20030 16737 3 A1	<input type="checkbox"/>	Method and system for reducing storage requirements for program code in a communication device	711/103
16	US 20030 15675 7 A1	<input type="checkbox"/>	Image processing apparatus and method for recognizing specific pattern and recording medium having image processing program recorded thereon	382/195
17	US 20030 14033 8 A1	<input type="checkbox"/>	Method, apparatus and article for generation of debugging information	717/162

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,539,911

DATED : July 23, 1996

INVENTOR(S): Nguyen *et al.*

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below.

In column 1, at line 36 insert therein:

—Page Printer Controller Including A Single Chip Superscalar Microprocessor With Graphics Functional Units, invented by Lentz *et al.*, Application Serial Number 08/267,646 filed June 28, 1994, now U.S. Patent No. 5,394,515, which is a continuation of 07/817,813, filed January 8, 1992, which is a continuation of 07/726,929, filed July 8, 1991; and—;

in column 14, at line 12, delete "So" and insert therein —to—; and

Column 44, line 28,
in Table III, at "reserved" row, move "0110" from middle column to last column, titled
"Instruction Symbol Condition Code".

Signed and Sealed this

Twenty-ninth Day of October 1996

Attest:



BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

	Docum ent ID	U	Title	Current OR
18	US 20030 13584 7 A1	<input type="checkbox"/>	Uninstrumenting in-line code instrumentation via stack unwinding and cleanup	717/158
19	US 20030 12659 0 A1	<input type="checkbox"/>	System and method for dynamic data-type checking	717/154
20	US 20030 12096 8 A1	<input type="checkbox"/>	Preserving dump capability after a fault-on-fault or related type failure in a fault tolerant computer system	714/25
21	US 20030 11557 3 A1	<input type="checkbox"/>	Efficient generic code in a dynamic execution environment	717/111
22	US 20030 09378 0 A1	<input type="checkbox"/>	Annotations to executable images for improved dynamic optimization of functions	717/153
23	US 20030 09354 5 A1	<input type="checkbox"/>	Method and system for downloading data to portable electronic device	709/231
24	US 20030 07920 2 A1	<input type="checkbox"/>	Exception handling in java computing environments	717/118
25	US 20030 07455 4 A1	<input type="checkbox"/>	Broadband interface unit and associated method	713/153
26	US 20030 07447 4 A1	<input type="checkbox"/>	Data distribution center and associated method	709/246
27	US 20030 07444 5 A1	<input type="checkbox"/>	Broadband network system and associated method	709/224
28	US 20030 04251 7 A1	<input type="checkbox"/>	Field-effect transistor having a contact to one of its doping regions, and method for fabricating the transistor	257/288
29	US 20030 02874 2 A1	<input type="checkbox"/>	METHOD FOR SECURING A TYPED DATA LANGUAGE, PARTICULARLY IN AN EMBEDDED SYSTEM, AND EMBEDDED SYSTEM FOR IMPLEMENTING THE METHOD	711/172
30	US 20030 02390 5 A1	<input type="checkbox"/>	Exception handling system and method	714/34
31	US 20030 01217 2 A1	<input type="checkbox"/>	Apparatus and method for transmitting a voice frame in an all-IP-based mobile communication system	370/342
32	US 20030 00645 0 A1	<input type="checkbox"/>	Two bit non-volatile electrically erasable and programmable memory structure, a process for producing said memory structure and methods for programming, reading and erasing said memory structure	257/316
33	US 20030 00521 2 A1	<input type="checkbox"/>	Method and apparatus for dynamically modifying a stored program	711/103
34	US 20020 19909 3 A1	<input type="checkbox"/>	Method and system for using internal FIFO RAM to improve system boot times	713/1

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,539,911

Page 1 of 3

DATED : July 23, 1996

INVENTOR(S) :
Nguyen *et al.*

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, in item [56], please add the cited references:

U.S. Patent 5,003,462, dated March 26, 1991, to Blaner *et al.*

U.S. Patent 4,942,525, dated July 17, 1990, to Shintani *et al.*

U.S. Patent 4,459,657, dated July 10, 1984, to Murao

U.S. Patent 4,434,641, dated February 28, 1984, to Puhl

U.S. Patent 4,410,939, dated October 18, 1983, to Kawakami

U.S. Patent 4,296,470, dated October 20, 1981, to Fairchild *et al.*

U.S. Patent 3,346,851, dated October 31, 1976 to Thornton *et al.*

European Patent EPA 0419105 A2, dated October 9, 1990

European Patent EPA 0402856, dated December 6, 1990

European Patent EPA 0377991 A3, dated December 20, 1989

European Patent EPA 0372751 A2, dated November 22, 1989

European Patent EPA 0136179 A2, dated September 27, 1984

French Patent 2575564, dated December 27, 1985

	Docum ent ID	U	Title	Current OR
35	US 20020 19445 9 A1	<input type="checkbox"/>	Method and apparatus for saving and restoring processor register values and allocating and deallocating stack memory	712/228
36	US 20020 18893 1 A1	<input type="checkbox"/>	Method for unwinding a program call stack	717/154
37	US 20020 15699 1 A1	<input type="checkbox"/>	Method and apparatus for 24-bit memory addressing in microcontrollers	711/219
38	US 20020 13881 9 A1	<input type="checkbox"/>	Computer programming language to describe and encapsulate a computer as a set of classes and objects	717/114
39	US 20020 12220 5 A1	<input type="checkbox"/>	Method of utilizing variable data fields with a page description language	358/1.1 5
40	US 20020 11220 3 A1	<input type="checkbox"/>	Fault handling in a data processing system utilizing a fault vector pointer table	714/48
41	US 20020 11220 2 A1	<input type="checkbox"/>	Fault vector pointer table	714/48
42	US 20020 10810 3 A1	<input type="checkbox"/>	Intercalling between native and non-native instruction sets	717/139
43	US 20020 08968 1 A1	<input type="checkbox"/>	Method of utilizing variable data fields with a page description language	358/1.1 1
44	US 20020 07571 9 A1	<input type="checkbox"/>	Low-cost three-dimensional memory array	365/130
45	US 20020 07283 0 A1	<input type="checkbox"/>	Dynamic classification of sections of software	701/1
46	US 20020 05956 0 A1	<input type="checkbox"/>	Debugging device and method	717/124
47	US 20020 04850 1 A1	<input type="checkbox"/>	Vehicle mounted large bale loading, transporting and unloading system	414/111
48	US 20020 04628 9 A1	<input type="checkbox"/>	Protocol stack for linking storage area networks over an existing LAN, MAN, or WAN Protocol stack for linking storage area networks over on existing , man, or wan	709/236
49	US 20020 04179 9 A1	<input type="checkbox"/>	Vehicle mounted large bale loading, transporting and unloading system	414/111
50	US 20020 03557 1 A1	<input type="checkbox"/>	Digital patent marking method	707/104 .1
51	US 20020 03280 4 A1	<input type="checkbox"/>	Heavyweight and lightweight instrumentation . . .	719/320

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,539,911

Page 2 of 3

DATED : July 23, 1996

INVENTOR(S) : Nguyen *et al.*

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

IEEE MICRO, vol. 9, no. 2, April 1989, Los Alamitos, CA, U.S., pages 26-38,

Charles Melear, Motorola, Inc., The Design of the 88000 RISC Family.

PATENT ABSTRACTS OF JAPAN, vol. 010, no. 089, April 1986, \$ JP, A, 60 225
943 (Hitachi Seisakusho K K) 11 November 1985.

IEEE TRANSACTIONS ON COMPUTERS, vol. 37, no. 5, may 1988, New
York, U.S., pages 562-573, J.E. Smith, A. R. Pleszkun, Implementing Precise
Interrupts in Pipelined Processors.

ELECTRO CONFERENCE RECORD, vol. 14, 11 April 1989, Los Angeles, U.S.
pages 511-519, Jelemensky, New Microcomputer Features Advanced Hardware
for Real-Time Control Applications.

COMPUTER DESIGN, vol. 28, no. 9, 1 May 1989, Littleton, Massachussetts,
U.S., pages 86-99, Andrews, Distinctions Blur Between DSP Solutions.

V. Popescu, M. Schultz, J. Spracklen, G. Gibson, B. Lightner & D. Isaman, The
Metaflow Architecture, Metaflow Technologies, Inc., June, 1991.

R. Weiss, "Third-Generation RISC Processors", On Special Report, March 30,
1992, pp. 96-108.

	Docum ent ID	U	Title	Current OR
52	US 20020 03271 8 A1	<input type="checkbox"/>	METHOD AND APPARATUS FOR MAINTAINING TRANSLATED ROUTINE STACK IN A BINARY TRANSLATION ENVIROMENT	718/107
53	US 20020 01390 7 A1	<input type="checkbox"/>	Method of preventing stack manipulation attacks during function calls	713/200
54	US 20010 05583 8 A1	<input type="checkbox"/>	Nonvolatile memory on SOI and compound semiconductor substrates and method of fabrication	438/129
55	US 20010 00759 2 A1	<input type="checkbox"/>	Biometric combination lock	382/116
56	US 67082 73 B1	<input type="checkbox"/>	Apparatus and method for implementing IPSEC transforms within an integrated circuit	713/189
57	US 67048 71 B1	<input type="checkbox"/>	Cryptographic co-processor	713/192
58	US 66979 59 B2	<input type="checkbox"/>	Fault handling in a data processing system utilizing a fault vector pointer table	714/10
59	US 66955 60 B2	<input type="checkbox"/>	Vehicle mounted large bale loading, transporting and unloading system	414/111
60	US 66912 19 B2	<input type="checkbox"/>	Method and apparatus for 24-bit memory addressing in microcontrollers	711/219
61	US 66878 45 B2	<input type="checkbox"/>	Fault vector pointer table	714/2
62	US 66870 16 B2	<input type="checkbox"/>	Method of utilizing variable data fields with a page description language	358/1.1 1
63	US 66657 93 B1	<input type="checkbox"/>	Method and apparatus for managing access to out-of-frame Registers	712/228
64	US 66434 00 B1	<input type="checkbox"/>	Image processing apparatus and method for recognizing specific pattern and recording medium having image processing program recorded thereon	382/195
65	US 66314 60 B1	<input type="checkbox"/>	Advanced load address table entry invalidation based on register address wraparound	712/217
66	US 66291 23 B1	<input type="checkbox"/>	Interception of unit creation requests by an automatic distributed partitioning system	718/106
67	US 65981 51 B1	<input type="checkbox"/>	Stack Pointer Management	712/228
68	US 65801 20 B2	<input type="checkbox"/>	Two bit non-volatile electrically erasable and programmable memory structure, a process for producing said memory structure and methods for programming, reading and erasing said memory structure	257/315
69	US 65500 58 B1	<input type="checkbox"/>	Stack clearing device and method	717/158
70	US 65499 59 B1	<input type="checkbox"/>	Detecting modification to computer memory by a DMA device	710/22
71	US 65359 03 B2	<input type="checkbox"/>	Method and apparatus for maintaining translated routine stack in a binary translation environment	718/100
72	US 65158 88 B2	<input type="checkbox"/>	Low cost three-dimensional memory array	365/130

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,539,911

Page 3 of 3

DATED : July 23, 1996

INVENTOR(S) : Nguyen *et al.*

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Johnson, Superscalar Microprocessor Design, Prentice-Hall, Inc., 1991, (in its entirety).

J. Hennessy & D. Patterson, Computer Architecture A Quantitative Approach, Morgan Kaufmann Publishers, Inc., 1990, (in its entirety).

Signed and Sealed this

Nineteenth Day of October, 1999

Attest:



Q. TODD DICKINSON

Attesting Officer

Acting Commissioner of Patents and Trademarks

	Docum ent ID	U	Title	Current OR
73	US 65022 37 B1	<input type="checkbox"/>	Method and apparatus for performing binary translation method and apparatus for performing binary translation	717/136
74	US 65021 81 B1	<input type="checkbox"/>	Method and apparatus for an enhanced processor	712/32
75	US 64991 37 B1	<input type="checkbox"/>	Reversible load-time dynamic linking	717/164
76	US 64907 21 B1	<input type="checkbox"/>	Software debugging method and apparatus	717/130
77	US 64839 11 B1	<input type="checkbox"/>	Methods and apparatus for providing external access to executable call flows of a network application	379/201 .03
78	US 64810 06 B1	<input type="checkbox"/>	Method and apparatus for efficient invocation of Java methods from native codes	717/139
79	US 64670 16 B1	<input type="checkbox"/>	Apparatus to record digital data on non-volatile memory card for recording in units of blocks of digital data and method thereof	711/103
80	US 64635 38 B1	<input type="checkbox"/>	Method of software protection using a random code generator	713/190
81	US 63973 79 B1	<input type="checkbox"/>	Recording in a program execution profile references to a memory-mapped active device	717/140
82	US 63895 40 B1	<input type="checkbox"/>	Stack based access control using code and executor identifiers	713/200
83	US 63817 35 B1	<input type="checkbox"/>	Dynamic classification of sections of software	717/158
84	US 63816 28 B1	<input type="checkbox"/>	Summarized application profiling and quick network profiling	709/201
85	US 63810 28 B1	<input type="checkbox"/>	Method of utilizing variable data fields with a page description language	358/1.1 1
86	US 63780 61 B1	<input type="checkbox"/>	Apparatus for issuing instructions and reissuing a previous instructions by recirculating using the delay circuit	712/200
87	US 63763 12 B1	<input type="checkbox"/>	Formation of non-volatile memory device comprised of an array of vertical field effect transistor structures	438/268
88	US 63739 67 B2	<input type="checkbox"/>	Biometric combination lock	382/115
89	US 63635 21 B1	<input type="checkbox"/>	Process for processing programs, process for detecting depth of frame associated with specified method, detection method, and computer	717/128
90	US 63634 74 B1	<input type="checkbox"/>	Process switching register replication in a data processing system	712/202
91	US 63453 83 B1	<input type="checkbox"/>	Debugging support device and debugging support method	717/124
92	US 63285 20 B1	<input type="checkbox"/>	Vehicle mounted large bale loading, transporting and unloading system	414/111
93	US 63178 69 B1	<input type="checkbox"/>	Method of run-time tracking of object references in Java programs	717/132
94	US 63145 13 B1	<input type="checkbox"/>	Method and apparatus for transferring data between a register stack and a memory resource	712/228
95	US 63016 99 B1	<input type="checkbox"/>	Method for detecting buffer overflow for computer security	717/131

	Document ID	U	Title	Current OR
96	US 63016 50 B1	<input type="checkbox"/>	Control unit and data processing system	712/35
97	US 62937 12 B1	<input type="checkbox"/>	Method and apparatus for constructing a stack unwind data structure	717/155
98	US 62827 00 B1	<input type="checkbox"/>	Mechanism for maintaining revisions of objects in flash memory	717/170
99	US 62726 13 B1	<input type="checkbox"/>	Method and system for accessing storage area of a digital data processing machine in both the physical and virtual addressing modes	711/204
100	US 62634 91 B1	<input type="checkbox"/>	Heavyweight and lightweight instrumentation	717/130
101	US 62634 01 B1	<input type="checkbox"/>	Method and apparatus for transferring data between a register stack and a memory resource	711/109
102	US 62471 70 B1	<input type="checkbox"/>	Method and data processing system for providing subroutine level instrumentation statistics	717/131
103	US 62303 12 B1	<input type="checkbox"/>	Automatic detection of per-unit location constraints	717/108
104	US 62299 06 B1	<input type="checkbox"/>	Biometric sequence codes	382/116
105	US 62267 89 B1	<input type="checkbox"/>	Method and apparatus for data flow analysis	717/138
106	US 62208 11 B1	<input type="checkbox"/>	Apparatus and method for handling and transporting bales	414/555
107	US 62196 66 B1	<input type="checkbox"/>	Autonomous transactions in a database system	707/8
108	US 62190 72 B1	<input type="checkbox"/>	Microcomputer with a built in character display circuit and visual display unit using such a microcomputer	345/531
109	US 62021 76 B1	<input type="checkbox"/>	Method of monitoring the correct execution of software programs	714/38
110	US 61991 56 B1	<input type="checkbox"/>	System for explicitly referencing a register for its current content when performing processor context switch	712/228
111	US 61990 95 B1	<input type="checkbox"/>	System and method for achieving object method transparency in a multi-code execution environment	718/107
112	US 61700 43 B1	<input type="checkbox"/>	Method for controlling an optic disk	711/158
113	US 61516 60 A	<input type="checkbox"/>	Information recording/reproducing apparatus having segmented cache memory	711/129
114	US 61515 69 A	<input type="checkbox"/>	Automated sequence of machine-performed attempts to unfreeze an apparently frozen application program	703/22
115	US 61382 72 A	<input type="checkbox"/>	GDMO translator, method of GDMO translation, and recording medium containing program for GDMO translator	717/142
116	US 61382 38 A	<input type="checkbox"/>	Stack-based access control using code and executor identifiers	713/200
117	US 61346 55 A	<input type="checkbox"/>	Method and apparatus for initializing a microprocessor to insure fault-free operation	713/1
118	US 61192 06 A	<input type="checkbox"/>	Design of tags for lookup of non-volatile registers	711/147

	Docum ent ID	U	Title	Current OR
119	US 61115 22 A	<input type="checkbox"/>	Multiple electronic purse parking meter	340/932 .2
120	US 61015 80 A	<input type="checkbox"/>	Apparatus and method for assisting exact garbage collection by using a stack cache of tag bits	711/132
121	US 60932 16 A	<input type="checkbox"/>	Method of run-time tracking of object references in Java programs	717/128
122	US 60918 97 A	<input type="checkbox"/>	Fast translation and execution of a computer program on a non-native architecture by use of background translator	717/138
123	US 60816 65 A	<input type="checkbox"/>	Method for efficient soft real-time execution of portable byte code computer programs	717/116
124	US 60700 57 A	<input type="checkbox"/>	System and method for improving reliability and performance of wireless communication systems using message pooling	455/67. 13
125	US 60554 14 A	<input type="checkbox"/>	System and method for improving reliability and performance of wireless communication systems using message pooling	455/67. 13
126	US 60386 11 A	<input type="checkbox"/>	Method for implementing a user-to-network (UNI) application programming interface (API)	719/328
127	US 60146 74 A	<input type="checkbox"/>	Method for maintaining log compatibility in database systems	707/202
128	US 60145 15 A	<input type="checkbox"/>	Enhanced stack unwind facility	717/129
129	US 60095 17 A	<input type="checkbox"/>	Mixed execution stack and exception handling	712/245
130	US 60092 58 A	<input type="checkbox"/>	Methods and devices for unwinding stack of frozen program and for restarting the program from unwound state	703/22
131	US 60000 28 A	<input type="checkbox"/>	Means and apparatus for maintaining condition codes in an unevaluated state	712/226
132	US 59830 18 A	<input type="checkbox"/>	Debug interrupt-handling microcomputer	717/127
133	US 59822 94 A	<input type="checkbox"/>	Paging receiver which performs data communication protocol analysis through execution of control program	340/7.4 4
134	US 59566 29 A	<input type="checkbox"/>	Method and apparatus for transmitter identification and selection for mobile information signal services	455/166 .2
135	US 59535 29 A	<input type="checkbox"/>	Data processor with a debug device and a stack area control unit and corresponding data processing method	717/135
136	US 59500 03 A	<input type="checkbox"/>	Profile instrumentation method and profile data collection method	717/130
137	US 59371 86 A	<input type="checkbox"/>	Asynchronous interrupt saving of prologue portions of computer programs	712/244
138	US 59371 53 A	<input type="checkbox"/>	Method of utilizing variable data fields with a page description language	358/1.1 7
139	US 59335 15 A	<input type="checkbox"/>	User identification through sequential input of fingerprints	382/124
140	US 59308 07 A	<input type="checkbox"/>	Apparatus and method for fast filtering read and write barrier operations in garbage collection system	707/206
141	US 59305 09 A	<input type="checkbox"/>	Method and apparatus for performing binary translation	717/159

	Document ID	U	Title	Current OR
142	US 59238 83 A	<input type="checkbox"/>	Optimization apparatus which removes transfer instructions by a global analysis of equivalence relations	717/156
143	US 59180 37 A	<input type="checkbox"/>	Generating tests for an extended finite state machine using different coverage levels for different submodels	716/2
144	US 59152 66 A	<input type="checkbox"/>	Processor core which provides a linear extension of an addressable memory space	711/211
145	US 59110 60 A	<input type="checkbox"/>	Computer method and apparatus for unfreezing an apparently frozen application program being executed under control of an operating system	718/100
146	US 59095 80 A	<input type="checkbox"/>	Development system and methods with direct compiler support for detecting invalid use and management of resources and memory at runtime	717/141
147	US 59095 79 A	<input type="checkbox"/>	Method and apparatus for encoding and decoding delta encoded information to locate live pointers in program data stacks	717/131
148	US 59077 09 A	<input type="checkbox"/>	Development system with methods for detecting invalid use and management of resources and memory at runtime	717/141
149	US 58999 85 A	<input type="checkbox"/>	Inference method and inference system	706/45
150	US 58931 21 A	<input type="checkbox"/>	System and method for swapping blocks of tagged stack entries between a tagged stack cache and an untagged main memory storage	707/206
151	US 58821 63 A	<input type="checkbox"/>	Front-end big bale loader	414/111
152	US 58570 96 A	<input type="checkbox"/>	Microarchitecture for implementing an instruction to clear the tags of a stack reference register file	712/229
153	US 58484 23 A	<input type="checkbox"/>	Garbage collection system and method for locating root set pointers in method activation records	707/206
154	US 58482 95 A	<input type="checkbox"/>	System for allocating common memory in cache such that data is maintained when exiting first programming structure and entering second programming structure	710/7
155	US 58420 17 A	<input type="checkbox"/>	Method and apparatus for forming a translation unit	717/158
156	US 58130 33 A	<input type="checkbox"/>	Superscalar microprocessor including a cache configured to detect dependencies between accesses to the cache and another cache	711/144
157	US 58070 53 A	<input type="checkbox"/>	Multiple hay bale transporter and loader	414/24.5
158	US 58058 74 A	<input type="checkbox"/>	Method and apparatus for performing a vector skip instruction in a data processor	712/222
159	US 58023 73 A	<input type="checkbox"/>	Method for providing a pipeline interpreter for a variable length instruction set	717/139
160	US 58022 67 A	<input type="checkbox"/>	Method for checkpointing in computer system under distributed processing environment	714/15
161	US 57874 74 A	<input type="checkbox"/>	Dependency checking structure for a pair of caches which are accessed from different pipeline stages of an instruction processing pipeline	711/138
162	US 57614 91 A	<input type="checkbox"/>	Data processing system and method for storing and restoring a stack pointer	712/244
163	US 57548 05 A	<input type="checkbox"/>	Instruction in a data processing system utilizing extension bits and method therefor	712/200
164	US 57547 59 A	<input type="checkbox"/>	Testing and monitoring of programmed devices	714/37

	Document ID	U	Title	Current OR
165	US 5752074 A	<input type="checkbox"/>	Data processing system and method thereof	712/29
166	US 5751988 A	<input type="checkbox"/>	Microcomputer with memory bank configuration and register bank configuration	711/5
167	US 5742786 A	<input type="checkbox"/>	Method and apparatus for storing vector data in multiple non-consecutive locations in a data processor using a mask value	711/217
168	US 5740443 A	<input type="checkbox"/>	Call-site specific selective automatic inlining	717/133
169	US 5737586 A	<input type="checkbox"/>	Data processing system and method thereof	712/236
170	US 5734879 A	<input type="checkbox"/>	Saturation instruction in a data processor	712/221
171	US 5732272 A	<input type="checkbox"/>	Subroutine execution time tracer	717/128
172	US 5729748 A	<input type="checkbox"/>	Call template builder and method	717/137
173	US 5729665 A	<input type="checkbox"/>	Method of utilizing variable data fields with a page description language	358/1.18
174	US 5717947 A	<input type="checkbox"/>	Data processing system and method thereof	712/3
175	US 5706488 A	<input type="checkbox"/>	Data processing system and method thereof	712/223
176	US 5675827 A	<input type="checkbox"/>	Information processing system, a processor, and an information processing method for the performing of an arithmetic operation of numeric information	715/538
177	US 5666510 A	<input type="checkbox"/>	Data processing device having an expandable address space	711/220
178	US 5664134 A	<input type="checkbox"/>	Data processor for performing a comparison instruction using selective enablement and wired boolean logic	712/245
179	US 5664060 A	<input type="checkbox"/>	Message management methods and apparatus	704/270
180	US 5647716 A	<input type="checkbox"/>	Tined, front-end big bale loader	414/111
181	US 5644709 A	<input type="checkbox"/>	Method for detecting computer memory access errors	714/53
182	US 5640541 A	<input type="checkbox"/>	Adapter for interfacing a SCSI bus with an IBM system/360/370 I/O interface channel and information system including same	703/26
183	US 5638517 A	<input type="checkbox"/>	Method and apparatus for transmitting a message from a computer system over a network adapter to the network by performing format conversion and memory verification	709/246
184	US 5636362 A	<input type="checkbox"/>	Programmable high watermark in stack frame cache using second region as a storage if first region is full and an event having a predetermined minimum priority	711/129
185	US 5618146 A	<input type="checkbox"/>	Hay roll transporter	414/24.5
186	US 5617532 A	<input type="checkbox"/>	Information processing apparatus and data back-up/restore system for the information processing apparatus	714/36
187	US 5600846 A	<input type="checkbox"/>	Data processing system and method thereof	712/5

	Document ID	U	Title	Current OR
188	US 55985 71 A	<input type="checkbox"/>	Data processor for conditionally modifying extension bits in response to data processing instruction execution	712/9
189	US 55862 93 A	<input type="checkbox"/>	Real time cache implemented by on-chip memory having standard and cache operating modes	711/118
190	US 55726 89 A	<input type="checkbox"/>	Data processing system and method thereof	712/200
191	US 55663 08 A	<input type="checkbox"/>	Processor core which provides a linear extension of an addressable memory space	711/2
192	US 55638 28 A	<input type="checkbox"/>	Method and apparatus for searching for data in multi-bit flash EEPROM memory arrays	365/185 .33
193	US 55599 73 A	<input type="checkbox"/>	Data processing system and method thereof	712/241
194	US 55510 39 A	<input type="checkbox"/>	Compiling a source code vector instruction by generating a subgrid loop for iteratively processing array elements by plural processing elements	717/150
195	US 55487 68 A	<input type="checkbox"/>	Data processing system and method thereof	712/200
196	US 55418 86 A	<input type="checkbox"/>	Method and apparatus for storing control information in multi-bit non-volatile memory arrays	365/185 .03
197	US 55375 62 A	<input type="checkbox"/>	Data processing system and method thereof	712/234
198	US 55195 17 A	<input type="checkbox"/>	Method and apparatus for holographically recording and reproducing images in a sequential manner	359/22
199	US 55049 22 A	<input type="checkbox"/>	Virtual machine with hardware display controllers for base and target machines	703/25
200	US 54756 93 A	<input type="checkbox"/>	Error management processes for flash EEPROM memory arrays	714/710

	L #	Hits	Search Text	DBs
1	L1	28267	stack near10 (frame area region space)	USPAT; US-PGPUB
2	L3	12095	stack near10 (frame area region space)	EPO; JPO; DERWENT; IBM_TDB
3	L4	74	(bit field tag flag cod\$3 encod\$3) near10 (sav\$3 stor\$3) near15 3	EPO; JPO; DERWENT; IBM_TDB
4	L2	285	(bit field tag flag cod\$3 encod\$3) near10 (sav\$3 stor\$3) near15 1	USPAT; US-PGPUB
5	L15	9164	(bit field tag flag) near10 instruction	EPO; JPO; DERWENT; IBM_TDB
6	L18	29308	(bit field tag flag) near10 instruction	USPAT; US-PGPUB
7	L17	34	(register near20 stack) near99 15	EPO; JPO; DERWENT; IBM_TDB
8	L23	443	(register near20 stack) near99 (18 near20 register)	USPAT; US-PGPUB

	Docum ent ID	U	Title	Current OR
1	JP 20002 84967 A	<input type="checkbox"/>	MICROCOMPUTER	
2	JP 10021 117 A	<input checked="" type="checkbox"/>	DEVICE AND METHOD FOR CONTROLLING PROGRAM EXECUTION	
3	JP 06095 958 A	<input checked="" type="checkbox"/>	DATA TABLE SYSTEM	
4	JP 05334 100 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
5	JP 05061 670 A	<input checked="" type="checkbox"/>	INTERRUPTION PROCESSING METHOD BASED UPON FLAG CONTROL	
6	JP 04052 962 A	<input checked="" type="checkbox"/>	ACCESS MASK CONTROL SYSTEM	
7	JP 04040 530 A	<input checked="" type="checkbox"/>	REAL TIME PROCESSOR	
8	JP 03083 737 A	<input checked="" type="checkbox"/>	FEEDER TRANSMISSION OF PAPER FACSIMILE MACHINE	
9	JP 03036 629 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
10	JP 02250 174 A	<input checked="" type="checkbox"/>	VECTOR PROCESSING DEVICE	
11	JP 62145 326 A	<input checked="" type="checkbox"/>	MICROPROGRAM CONTROL CIRCUIT	
12	JP 62044 836 A	<input checked="" type="checkbox"/>	MICROADDRESS STACK CONTROL SYSTEM	
13	JP 62025 333 A	<input checked="" type="checkbox"/>	MICROCOMPUTER	
14	JP 61289 430 A	<input checked="" type="checkbox"/>	MICROCOMPUTER	
15	JP 61188 628 A	<input checked="" type="checkbox"/>	INSTRUCTION PROCESSING AND CONTROLLER SYSTEM IN INFORMATION PROCESSOR	
16	JP 61148 533 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
17	JP 61101 838 A	<input checked="" type="checkbox"/>	INSTRUCTION DECODE SYSTEM	
18	JP 61082 244 A	<input checked="" type="checkbox"/>	INTER-TASK DATA TRANSMITTING AND RECEIVING SYSTEM	
19	JP 61032 148 A	<input checked="" type="checkbox"/>	DESIGNATION INSTRUCTION TRACE SYSTEM	
20	JP 55115 155 A	<input checked="" type="checkbox"/>	ONE CHIP MULTI-MICROCOMPUTER	
21	EP 36317 4 A2	<input checked="" type="checkbox"/>	Branch on bit processing.	
22	NN860 44737	<input checked="" type="checkbox"/>	Indirect Program Access for a Signal Processor	

	Docum ent ID	U	Title	Current OR
23	US 20020 19445 9 A	<input checked="" type="checkbox"/>	Instruction encoding method for data processing system, involves storing register value as argument or static value in stack memory location set by calling or called program, based on encoded field	
24	US 59789 01 A	<input checked="" type="checkbox"/>	Floating point and multimedia unit with instruction reclassifier for superscalar processor	
25	EP 93128 6 A	<input checked="" type="checkbox"/>	Stack oriented architecture for microprocessor	
26	US 58125 62 A	<input checked="" type="checkbox"/>	VLSIC operating method for testing and debugging purpose - involves shifting control values which includes stop clock flag request bit into control register while system clock is provided to function block	
27	US 57908 54 A	<input checked="" type="checkbox"/>	Vector data processor for fuzzy logic - involves retrieving specific value from stack and stored as current Vt bit mask, if conditional statement is false	
28	EP 36388 9 A	<input checked="" type="checkbox"/>	Vector processor vector data prepn. - has buffer in memory controller storing vector data in response to decoder request signal	
29	EP 36317 4 A	<input checked="" type="checkbox"/>	Detection branch on bit unit for data processing system - provides branching on variable branch condition or status parameters selectable by program instructions	
30	EP 35208 2 A	<input checked="" type="checkbox"/>	Operating memory stack in high-speed CPU - unconditionally writing from write bus to register of pointed to stack, and copying contents of register to read bus	
31	EP 18479 1 A	<input checked="" type="checkbox"/>	Information processor carrying out vector calculation - has state indication unit producing flags representing internal states of instruction processing unit	
32	EP 12612 4 A	<input checked="" type="checkbox"/>	Pipelined micro-controller with multiple store access for clock cycle - has microinstructions comprising jump address, control and instruction fields to handle nested subroutines	
33	EP 10667 1 A	<input checked="" type="checkbox"/>	Pre-etching instructions for multi-staged or pipe-lined CPU - using transfer and indirect prediction table predicting target address of transfer and indirect instructions based on history of execution	
34	EP 74479 A	<input type="checkbox"/>	Data processor with architecture - permits inter-segment programme calls with associated selective allocation of data segments of varying length	

	Document ID	U	Title	Current OR
1	US 20040 05989 5 A1	<input type="checkbox"/>	Microprocessor circuit for portable data carriers and method for operating the circuit	712/223
2	US 20040 04249 0 A1	<input checked="" type="checkbox"/>	State record processing	370/469
3	US 20040 01567 8 A1	<input checked="" type="checkbox"/>	Microprocessor for executing byte compiled Java code	712/202
4	US 20040 00668 7 A1	<input checked="" type="checkbox"/>	Processor and instruction control method	712/220
5	US 20040 00668 5 A1	<input checked="" type="checkbox"/>	Processor and instruction control method	712/218
6	US 20030 23163 4 A1	<input checked="" type="checkbox"/>	Table driven programming system for a services processor	370/395 .32
7	US 20030 21719 9 A1	<input checked="" type="checkbox"/>	Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure	710/1
8	US 20030 21287 8 A1	<input checked="" type="checkbox"/>	Scaleable microprocessor architecture	712/23
9	US 20030 20041 9 A1	<input checked="" type="checkbox"/>	Non-copy shared stack and register file device and dual language processor structure using the same	712/202
10	US 20030 19394 9 A1	<input checked="" type="checkbox"/>	Packet processing device	370/392
11	US 20030 19192 9 A1	<input checked="" type="checkbox"/>	Microinstruction pointer stack in a processor	712/245
12	US 20030 18812 8 A1	<input checked="" type="checkbox"/>	Executing stack-based instructions within a data processing apparatus arranged to apply operations to data items stored in registers	712/202
13	US 20030 17734 2 A1	<input checked="" type="checkbox"/>	Processor with register dirty bits and special save multiple/return instructions	712/228
14	US 20030 17733 7 A1	<input checked="" type="checkbox"/>	Computer system	712/202
15	US 20030 15207 8 A1	<input checked="" type="checkbox"/>	Services processor having a packet editing unit	370/389
16	US 20030 13584 4 A1	<input checked="" type="checkbox"/>	Bytecode program interpreter apparatus and method with pre-verification of data type restrictions and object initialization	717/126
17	US 20030 13571 9 A1	<input checked="" type="checkbox"/>	Method and system using hardware assistance for tracing instruction disposition information	712/227

	Document ID	U	Title	Current OR
18	US 20030 12090 3 A1	<input checked="" type="checkbox"/>	Load/move and duplicate instructions for a processor	712/221
19	US 20030 10579 3 A1	<input checked="" type="checkbox"/>	Long instruction word controlling plural independent processor operations	708/625
20	US 20030 02390 5 A1	<input checked="" type="checkbox"/>	Exception handling system and method	714/34
21	US 20030 01868 1 A1	<input checked="" type="checkbox"/>	System and method for recovering applications	718/102
22	US 20020 19445 9 A1	<input checked="" type="checkbox"/>	Method and apparatus for saving and restoring processor register values and allocating and deallocating stack memory	712/228
23	US 20020 17971 9 A1	<input checked="" type="checkbox"/>	Selective access to multiple registers having a common name	235/492
24	US 20020 15700 0 A1	<input checked="" type="checkbox"/>	Software hint to improve the branch target prediction accuracy	712/239
25	US 20020 14409 1 A1	<input checked="" type="checkbox"/>	Method and apparatus for dynamic register management in a processor	712/217
26	US 20020 13871 5 A1	<input checked="" type="checkbox"/>	Microprocessor executing data transfer between memory and register and data transfer between registers in response to single push/pop instruction	712/225
27	US 20020 13871 2 A1	<input checked="" type="checkbox"/>	Data processing device with instruction translator and memory interface device	712/205
28	US 20020 12922 5 A1	<input checked="" type="checkbox"/>	Processing device for executing virtual machine instructions	712/227
29	US 20020 10399 1 A1	<input checked="" type="checkbox"/>	Multi-cycle instructions	712/219
30	US 20020 09766 7 A1	<input checked="" type="checkbox"/>	Cyclic buffer for infrared	370/205
31	US 20020 06600 4 A1	<input checked="" type="checkbox"/>	Storing stack operands in registers	712/209
32	US 20020 05461 2 A1	<input checked="" type="checkbox"/>	Integrated circuit configurations and methods for providing functions for public telephones	370/535
33	US 20020 04637 2 A1	<input checked="" type="checkbox"/>	SEQUENCE CONTROL CIRCUIT	714/718
34	US 20020 04290 9 A1	<input checked="" type="checkbox"/>	Retargetable compiling system and method	717/149

	Docum ent ID	U	Title	Current OR
35	US 20010 04486 6 A1	<input checked="" type="checkbox"/>	Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure	710/305
36	US 20010 03229 6 A1	<input checked="" type="checkbox"/>	Data processor	711/128
37	US 20010 01007 2 A1	<input checked="" type="checkbox"/>	Instruction translator translating non-native instructions for a processor into native instructions therefor, instruction memory with such translator, and data processing apparatus using them	712/209
38	US 66913 06 B1	<input checked="" type="checkbox"/>	Use of limited program space of general purpose processor for unlimited sequence of translated instructions	717/139
39	US 66663 83 B2	<input checked="" type="checkbox"/>	Selective access to multiple registers having a common name	235/492
40	US 66657 93 B1	<input checked="" type="checkbox"/>	Method and apparatus for managing access to out-of-frame Registers	712/228
41	US 66584 71 B1	<input checked="" type="checkbox"/>	Method and system for zero overhead software performance measurement instrumentation	709/224
42	US 66549 34 B1	<input checked="" type="checkbox"/>	Programmable event engine	716/4
43	US 66511 59 B1	<input checked="" type="checkbox"/>	Floating point register stack management for CISC	712/209
44	US 66339 74 B1	<input checked="" type="checkbox"/>	Apparatus and method for controlling link stack corruption during speculative instruction branching using multiple stacks	712/237
45	US 66153 00 B1	<input checked="" type="checkbox"/>	Fast look-up of indirect branch destination in a dynamic translation system	710/100
46	US 66041 90 B1	<input checked="" type="checkbox"/>	Data address prediction structure and a method for operating the same	712/207
47	US 65981 49 B1	<input checked="" type="checkbox"/>	Performance enhancement for code transitions of floating point and packed data modes	712/222
48	US 65981 48 B1	<input checked="" type="checkbox"/>	High performance microprocessor having variable speed system clock	712/32
49	US 65879 10 B2	<input checked="" type="checkbox"/>	Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure	710/306
50	US 65804 56 B1	<input checked="" type="checkbox"/>	Programmable timing generator	348/312
51	US 65747 28 B1	<input checked="" type="checkbox"/>	Condition code stack architecture systems and methods	712/234
52	US 65679 33 B1	<input checked="" type="checkbox"/>	Emulation suspension mode with stop mode extension	714/31
53	US 65643 39 B1	<input checked="" type="checkbox"/>	Emulation suspension mode handling multiple stops and starts	714/30
54	US 65606 92 B1	<input checked="" type="checkbox"/>	Data processing circuit, microcomputer, and electronic equipment	712/23
55	US 65571 16 B1	<input checked="" type="checkbox"/>	Emulation suspension mode with frame controlled resource access	714/28
56	US 65535 13 B1	<input checked="" type="checkbox"/>	Emulation suspend mode with differing response to differing classes of interrupts	714/28

	Docum ent ID	U	Title	Current OR
57	US 65265 03 B1	<input checked="" type="checkbox"/>	Apparatus and method for accessing a memory device during speculative instruction branching	712/242
58	US 65196 96 B1	<input checked="" type="checkbox"/>	Paired register exchange using renaming register map	712/222
59	US 65079 04 B1	<input checked="" type="checkbox"/>	Executing isolated mode instructions in a secure system running in privilege rings	712/229
60	US 64777 02 B1	<input checked="" type="checkbox"/>	Bytecode program interpreter apparatus and method with pre-verification of data type restrictions and object initialization	717/126
61	US 64497 09 B1	<input checked="" type="checkbox"/>	Fast stack save and restore system and method	712/202
62	US 64426 73 B1	<input checked="" type="checkbox"/>	Update forwarding cache for address mode	712/202
63	US 64306 70 B1	<input checked="" type="checkbox"/>	Apparatus and method for a virtual hashed page table	711/216
64	US 64217 73 B1	<input checked="" type="checkbox"/>	Sequence control circuit	712/234
65	US 64089 85 B1	<input checked="" type="checkbox"/>	Motor driven lubricator	184/37
66	US 64083 20 B1	<input checked="" type="checkbox"/>	Instruction set architecture with versatile adder carry control	708/518
67	US 64053 05 B1	<input checked="" type="checkbox"/>	Rapid execution of floating point load control word instructions	712/222
68	US 63935 49 B1	<input checked="" type="checkbox"/>	Instruction alignment unit for routing variable byte-length instructions	712/204
69	US 63705 58 B1	<input checked="" type="checkbox"/>	Long instruction word controlling plural independent processor operations	708/603
70	US 63670 05 B1	<input checked="" type="checkbox"/>	System and method for synchronizing a register stack engine (RSE) and backing memory image with a processor's execution of instructions during a state saving context switch	712/228
71	US 63493 77 B1	<input checked="" type="checkbox"/>	Processing device for executing virtual machine instructions that includes instruction refeeding means	712/22
72	US 63381 34 B1	<input checked="" type="checkbox"/>	Method and system in a superscalar data processing system for the efficient processing of an instruction by moving only pointers to data	712/217
73	US 63321 87 B1	<input checked="" type="checkbox"/>	Cumulative lookahead to eliminate chained dependencies	712/23
74	US 63145 13 B1	<input checked="" type="checkbox"/>	Method and apparatus for transferring data between a register stack and a memory resource	712/228
75	US 63016 50 B1	<input checked="" type="checkbox"/>	Control unit and data processing system	712/35
76	US 62984 34 B1	<input checked="" type="checkbox"/>	Data processing device for processing virtual machine instructions	712/209
77	US 62929 35 B1	<input checked="" type="checkbox"/>	Method for fast translation of java byte codes into efficient native processor code	717/148
78	US 62928 44 B1	<input checked="" type="checkbox"/>	Media storage device with embedded data filter for dynamically processing data during read and write operations	710/5
79	US 62894 17 B1	<input checked="" type="checkbox"/>	Operand supply to an execution unit	711/131

	Docum ent ID	U	Title	Current OR
80	US 62725 96 B1	<input checked="" type="checkbox"/>	Data processor	711/128
81	US 62694 36 B1	<input checked="" type="checkbox"/>	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
82	US 62667 27 B1	<input checked="" type="checkbox"/>	Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure	710/105
83	US 62567 25 B1	<input checked="" type="checkbox"/>	Shared datapath processor utilizing stack-based and register-based storage spaces	712/200
84	US 62567 21 B1	<input checked="" type="checkbox"/>	Register renaming in which moves are accomplished by swapping tags	712/23
85	US 62471 71 B1	<input checked="" type="checkbox"/>	Bytecode program interpreter apparatus and method with pre-verification of a data type restrictions and object initialization	717/126
86	US 62405 03 B1	<input checked="" type="checkbox"/>	Cumulative lookahead to eliminate chained dependencies	712/23
87	US 62404 37 B1	<input checked="" type="checkbox"/>	Long instruction word controlling plural independent processor operations	708/524
88	US 62370 83 B1	<input checked="" type="checkbox"/>	Microprocessor including multiple register files mapped to the same logical storage and inhibiting sychronization between the register files responsive to inclusion of an instruction in an instruction sequence	712/217
89	US 62336 72 B1	<input checked="" type="checkbox"/>	Piping rounding mode bits with floating point instructions to eliminate serialization	712/222
90	US 62336 37 B1	<input checked="" type="checkbox"/>	Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure	710/311
91	US 62197 83 B1	<input checked="" type="checkbox"/>	Method and apparatus for executing a flush RS instruction to synchronize a register stack with instructions executed by a processor	712/228
92	US 62196 88 B1	<input checked="" type="checkbox"/>	Method, apparatus and system for sum of plural absolute differences	708/709
93	US 62162 14 B1	<input checked="" type="checkbox"/>	Apparatus and method for a virtual hashed page table	711/207
94	US 62090 82 B1	<input checked="" type="checkbox"/>	Apparatus and method for optimizing execution of push all/pop all instructions	712/225
95	US 62055 41 B1	<input checked="" type="checkbox"/>	System and method using selection logic units to define stack orders	712/217
96	US 62052 23 B1	<input checked="" type="checkbox"/>	Input data format autodetection systems and methods	380/42
97	US 61890 68 B1	<input checked="" type="checkbox"/>	Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle	711/3
98	US 61856 29 B1	<input checked="" type="checkbox"/>	Data transfer controller employing differing memory interface protocols dependent upon external input at predetermined time	710/10
99	US 61733 94 B1	<input checked="" type="checkbox"/>	Instruction having bit field designating status bits protected from modification corresponding to arithmetic logic unit result	712/226
100	US 61733 05 B1	<input checked="" type="checkbox"/>	Division by iteration employing subtraction and conditional source selection of a prior difference or a left shifted remainder	708/650
101	US 61345 73 A	<input checked="" type="checkbox"/>	Apparatus and method for absolute floating point register addressing	708/510

	Docum ent ID	U	Title	Current OR
102	US 61167 68 A	<input checked="" type="checkbox"/>	Three input arithmetic logic unit with barrel rotator	708/236
103	US 61157 77 A	<input checked="" type="checkbox"/>	LOADRS instruction and asynchronous context switch	710/260
104	US 61122 96 A	<input checked="" type="checkbox"/>	Floating point stack manipulation using a register map and speculative top of stack values	712/222
105	US 61122 92 A	<input checked="" type="checkbox"/>	Code sequence for asynchronous backing store switch utilizing both the cover and LOADRS instructions	712/200
106	US 61120 18 A	<input checked="" type="checkbox"/>	Apparatus for exchanging two stack registers	712/202
107	US 60981 67 A	<input checked="" type="checkbox"/>	Apparatus and method for fast unified interrupt recovery and branch recovery in processors supporting out-of-order execution	712/218
108	US 60981 63 A	<input checked="" type="checkbox"/>	Three input arithmetic logic unit with shifter	712/20
109	US 60947 16 A	<input checked="" type="checkbox"/>	Register renaming in which moves are accomplished by swapping rename tags	712/23
110	US 60817 83 A	<input checked="" type="checkbox"/>	Dual processor digital audio decoder with shared memory data transfer and task partitioning for decompressing compressed audio data, and systems and methods using the same	704/500
111	US 60790 08 A	<input checked="" type="checkbox"/>	Multiple thread multiple data predictive coded parallel processing system and method	712/11
112	US 60790 06 A	<input checked="" type="checkbox"/>	Stride-based data address prediction structure	711/213
113	US 60702 52 A	<input checked="" type="checkbox"/>	Method and apparatus for interactive built-in-self-testing with user-programmable test patterns	714/30
114	US 60676 13 A	<input checked="" type="checkbox"/>	Rotation register for orthogonal data transformation	712/32
115	US 60651 14 A	<input checked="" type="checkbox"/>	Cover instruction and asynchronous backing store switch	712/228
116	US 60617 85 A	<input checked="" type="checkbox"/>	Data processing system having an apparatus for out-of-order register operations and method therefor	712/236
117	US 60617 11 A	<input checked="" type="checkbox"/>	Efficient context saving and restoring in a multi-tasking computing system environment	718/108
118	US 60584 73 A	<input checked="" type="checkbox"/>	Memory store from a register pair conditional upon a selected status bit	712/225
119	US 60584 67 A	<input checked="" type="checkbox"/>	Standard cell, 4-cycle, 8-bit microcontroller	712/32
120	US 60556 19 A	<input checked="" type="checkbox"/>	Circuits, system, and methods for processing multiple data streams	712/36
121	US 60321 70 A	<input checked="" type="checkbox"/>	Long instruction word controlling plural independent processor operations	708/620
122	US 60264 84 A	<input checked="" type="checkbox"/>	Data processing apparatus, system and method for if, then, else operation using write priority	712/226
123	US 60187 98 A	<input checked="" type="checkbox"/>	Floating point unit using a central window for storing instructions capable of executing multiple instructions in a single clock cycle	712/220
124	US 60165 44 A	<input checked="" type="checkbox"/>	Apparatus and method for tracking changes in address size and for different size retranslate second instruction with an indicator from address size	712/234

	Docum ent ID	U	Title	Current OR
125	US 60165 38 A	<input checked="" type="checkbox"/>	Method, apparatus and system forming the sum of data in plural equal sections of a single data word	712/32
126	US 60147 34 A	<input checked="" type="checkbox"/>	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
127	US 60121 28 A	<input checked="" type="checkbox"/>	Microcontroller having a page address mode	711/163
128	US 60095 11 A	<input checked="" type="checkbox"/>	Apparatus and method for tagging floating point operands and results for rapid detection of special floating point numbers	712/222
129	US 60095 09 A	<input checked="" type="checkbox"/>	Method and system for the temporary designation and utilization of a plurality of physical registers as a stack	712/202
130	US 60063 24 A	<input checked="" type="checkbox"/>	High performance superscalar alignment unit	712/204
131	US 60031 34 A	<input checked="" type="checkbox"/>	Secure open smart card architecture	713/200
132	US 60031 28 A	<input checked="" type="checkbox"/>	Number of pipeline stages and loop length related counter differential based end-loop prediction	712/241
133	US 59997 31 A	<input checked="" type="checkbox"/>	Bytecode program interpreter apparatus and method with pre-verification of data type restrictions and object initialization	717/126
134	US 59957 48 A	<input checked="" type="checkbox"/>	Three input arithmetic logic unit with shifter and/or mask generator	712/221
135	US 59957 47 A	<input checked="" type="checkbox"/>	Three input arithmetic logic unit capable of performing all possible three operand boolean operations with shifter and/or mask generator	712/221
136	US 59875 96 A	<input checked="" type="checkbox"/>	Register rename stack for a microprocessor	712/217
137	US 59875 61 A	<input checked="" type="checkbox"/>	Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle	711/3
138	US 59833 28 A	<input checked="" type="checkbox"/>	Data processing device with time-multiplexed memory bus	711/157
139	US 59833 07 A	<input checked="" type="checkbox"/>	Electrical circuit for exchanging data between a microprocessor and a memory and computer comprising a circuit of this type	710/310
140	US 59789 07 A	<input checked="" type="checkbox"/>	Delayed update register for an array	712/239
141	US 59789 01 A	<input checked="" type="checkbox"/>	Floating point and multimedia unit with data type reclassification capability	712/222
142	US 59788 25 A	<input checked="" type="checkbox"/>	Zero detection circuitry and methods	708/525
143	US 59745 39 A	<input checked="" type="checkbox"/>	Three input arithmetic logic unit with shifter and mask generator	712/221
144	US 59745 33 A	<input checked="" type="checkbox"/>	Data processor	712/211
145	US 59744 32 A	<input checked="" type="checkbox"/>	On-the-fly one-hot encoding of leading zero count	708/205
146	US 59681 69 A	<input checked="" type="checkbox"/>	Superscalar microprocessor stack structure for judging validity of predicted subroutine return addresses	712/239
147	US 59616 35 A	<input checked="" type="checkbox"/>	Three input arithmetic logic unit with barrel rotator and mask generator	712/221

	Docum ent ID	U	Title	Current OR
148	US 59601 93 A	<input checked="" type="checkbox"/>	Apparatus and system for sum of plural absolute differences	712/221
149	US 59499 96 A	<input checked="" type="checkbox"/>	Processor having a variable number of stages in a pipeline	712/244
150	US 59448 12 A	<input checked="" type="checkbox"/>	Register rename stack for a microprocessor	712/23
151	US 59448 01 A	<input checked="" type="checkbox"/>	Isochronous buffers for MMx-equipped microprocessors	710/29
152	US 59403 11 A	<input checked="" type="checkbox"/>	Immediate floating-point operand reformatting in a microprocessor	708/204
153	US 59352 39 A	<input checked="" type="checkbox"/>	Parallel mask decoder and method for generating said mask	712/224
154	US 59336 18 A	<input checked="" type="checkbox"/>	Speculative register storage for storing speculative results corresponding to register updated by a plurality of concurrently recorded instruction	712/217
155	US 59319 43 A	<input checked="" type="checkbox"/>	Floating point NaN comparison	712/222
156	US 59304 92 A	<input checked="" type="checkbox"/>	Rapid pipeline control using a control word and a steering word	712/216
157	US 59220 68 A	<input checked="" type="checkbox"/>	Information processing system and information processing method for executing instructions in parallel	712/215
158	US 59139 24 A	<input checked="" type="checkbox"/>	Use of a stored signal to switch between memory banks	711/212
159	US 59130 48 A	<input checked="" type="checkbox"/>	Dispatching instructions in a processor supporting out-of-order execution	712/215
160	US 59130 47 A	<input checked="" type="checkbox"/>	Pairing floating point exchange instruction with another floating point instruction to reduce dispatch latency	712/213
161	US 59095 67 A	<input checked="" type="checkbox"/>	Apparatus and method for native mode processing in a RISC-based CISC processor	712/208
162	US 59078 64 A	<input checked="" type="checkbox"/>	Data processing device with time-multiplexed memory bus	711/169
163	US 58954 97 A	<input checked="" type="checkbox"/>	Microprocessor with pipelining, memory size evaluation, micro-op code and tags	711/169
164	US 58929 36 A	<input checked="" type="checkbox"/>	Speculative register file for storing speculative register states and removing dependencies between instructions utilizing the register	712/216
165	US 58871 85 A	<input checked="" type="checkbox"/>	Interface for coupling a floating point unit to a reorder buffer	712/23
166	US 58871 61 A	<input checked="" type="checkbox"/>	Issuing instructions in a processor supporting out-of-order execution	712/244
167	US 58871 52 A	<input checked="" type="checkbox"/>	Load/store unit with multiple oldest outstanding instruction pointers for completing store and load/store miss instructions	712/217
168	US 58840 62 A	<input checked="" type="checkbox"/>	Microprocessor with pipeline status integrity logic for handling multiple stage writeback exceptions	712/218
169	US 58813 05 A	<input checked="" type="checkbox"/>	Register rename stack for a microprocessor	712/23
170	US 58812 78 A	<input checked="" type="checkbox"/>	Return address prediction system which adjusts the contents of return stack storage to enable continued prediction after a mispredicted branch	712/242

	Docum ent ID	U	Title	Current OR
171	US 58782 55 A	<input checked="" type="checkbox"/>	Update unit for providing a delayed update to a branch prediction array	712/240
172	US 58753 24 A	<input checked="" type="checkbox"/>	Superscalar microprocessor which delays update of branch prediction information in response to branch misprediction until a subsequent idle clock	712/238
173	US 58753 15 A	<input checked="" type="checkbox"/>	Parallel and scalable instruction scanning unit	712/204
174	US 58647 07 A	<input checked="" type="checkbox"/>	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
175	US 58601 04 A	<input checked="" type="checkbox"/>	Data cache which speculatively updates a predicted data cache storage location with store data and subsequently corrects mispredicted updates	711/137
176	US 58599 91 A	<input checked="" type="checkbox"/>	Parallel and scalable method for identifying valid instructions and a superscalar microprocessor including an instruction scanning unit employing the method	712/204
177	US 58570 96 A	<input checked="" type="checkbox"/>	Microarchitecture for implementing an instruction to clear the tags of a stack reference register file	712/229
178	US 58549 21 A	<input checked="" type="checkbox"/>	Stride-based data address prediction structure	712/239
179	US 58527 26 A	<input checked="" type="checkbox"/>	Method and apparatus for executing two types of instructions that specify registers of a shared logical register file in a stack and a non-stack referenced manner	712/200
180	US 58505 43 A	<input checked="" type="checkbox"/>	Microprocessor with speculative instruction pipelining storing a speculative register value within branch target buffer for use in speculatively executing instructions after a return	712/238
181	US 58484 33 A	<input checked="" type="checkbox"/>	Way prediction unit and a method for operating the same	711/137
182	US 58359 73 A	<input checked="" type="checkbox"/>	Instruction processing unit capable of efficiently accessing the entire address space of an external memory	711/220
183	US 58359 67 A	<input checked="" type="checkbox"/>	Adjusting prefetch size based on source of prefetch address	711/213
184	US 58359 51 A	<input checked="" type="checkbox"/>	Branch processing unit with target cache read prioritization protocol for handling multiple hits	711/145
185	US 58322 97 A	<input checked="" type="checkbox"/>	Superscalar microprocessor load/store unit employing a unified buffer and separate pointers for load and store operations	710/5
186	US 58322 49 A	<input checked="" type="checkbox"/>	High performance superscalar alignment unit	712/204
187	US 58260 71 A	<input checked="" type="checkbox"/>	Parallel mask decoder and method for generating said mask	712/224
188	US 58260 57 A	<input checked="" type="checkbox"/>	Method for managing virtual address space at improved space utilization efficiency	703/24
189	US 58225 74 A	<input checked="" type="checkbox"/>	Functional unit with a pointer for mispredicted resolution, and a superscalar microprocessor employing the same	712/233
190	US 58225 59 A	<input checked="" type="checkbox"/>	Apparatus and method for aligning variable byte-length instructions to a plurality of issue positions	712/214
191	US 58225 58 A	<input checked="" type="checkbox"/>	Method and apparatus for predecoding variable byte-length instructions within a superscalar microprocessor	712/213
192	US 58190 59 A	<input checked="" type="checkbox"/>	Predecode unit adapted for variable byte-length instruction set processors and method of operating the same	712/213

	Docum ent ID	U	Title	Current OR
193	US 58190 57 A	<input checked="" type="checkbox"/>	Superscalar microprocessor including an instruction alignment unit with limited dispatch to decode units	712/204
194	US 58130 33 A	<input checked="" type="checkbox"/>	Superscalar microprocessor including a cache configured to detect dependencies between accesses to the cache and another cache	711/144
195	US 58128 13 A	<input checked="" type="checkbox"/>	Apparatus and method for of register changes during execution of a micro instruction tracking sequence	712/218
196	US 58125 62 A	<input checked="" type="checkbox"/>	Low cost emulation scheme implemented via clock control using JTAG controller in a scan environment	714/726
197	US 58092 74 A	<input checked="" type="checkbox"/>	Purge control for ON-chip cache memory	712/210
198	US 58059 13 A	<input checked="" type="checkbox"/>	Arithmetic logic unit with conditional register source selection	712/209
199	US 57908 54 A	<input checked="" type="checkbox"/>	Efficient stack utilization for compiling and executing nested if-else constructs in a vector data processing system	717/150
200	US 57874 74 A	<input checked="" type="checkbox"/>	Dependency checking structure for a pair of caches which are accessed from different pipeline stages of an instruction processing pipeline	711/138